and a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit; and

driving the second drive circuit to generate a second output signal having the first state after the first output signal is changed by a predetermined amount by the first drive circuit.

2. (Twice Amended) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor connected between a first power supply and an output terminal of the output buffer circuit and a second output transistor connected between a second power supply and the output terminal, the second drive circuit including a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating a first output signal having a first state in accordance with the input signal using the first drive circuit;

generating a delay signal by delaying the output signal;

generating a control signal for controlling the third and fourth output transistors in accordance with the delay signal and the input signal; and

driving the second drive circuit to generate a second output signal having the first state after the first output signal is changed by a predetermined amount by the first drive circuit.

3. (Once Amended) The method according to claim 2, wherein the first output signal generating step includes generating the first output signal by turning on the first output transistor;

the driving step includes turning on the third output transistor with the control signal; and

the method further comprises step of substantially simultaneously turning off the first and third output transistors in accordance with a change in the input signal.

4. (Once Amended) The method according to claim 2, wherein the first output signal generating step includes generating the first output signal by turning on the second output transistor;

the driving step includes turning on the fourth output transistor with the control signal; and

the method further comprises a step of substantially simultaneously turning off the second and fourth output transistors in accordance with a change in the input signal.

5. (Twice Amended) An output buffer circuit comprising:

a first drive circuit, connected to an output terminal, for receiving an input signal and generating a first output signal having a first state;

a second drive circuit connected to the output terminal and having a lower output impedance than the first drive circuit, wherein the second drive circuit generates a second output signal having the first state; and

a first control circuit, connected to the second drive circuit, for generating a first control signal for driving the second drive circuit on the basis of the input signal and the first output signal after the first output signal is changed by a predetermined amount by the first drive circuit.

6. (Once Amended) The output buffer circuit according to claim 5, wherein the first drive circuit includes a first output transistor connected between a first power supply and the output terminal and a second output transistor connected between a second power supply and the output terminal, wherein the first and second output transistors generate the first output signal; and

the second drive circuit includes a third output transistor connected between the first power supply and the output terminal and a fourth output transistor connected between the second power supply and the output terminal, the third and fourth output transistors having lower impedances than the first and second output transistors.

7. (Once Amended) The output buffer circuit according to claim 6, wherein the first control circuit turns on the third output transistor with the first control signal after the first output transistor is turned on by the input signal, and the first control circuit turns on the fourth output transistor with the first control signal after the second output transistor is turned on by the input signal.

11. (Once Amended) The output buffer circuit according to claim 10, wherein the first control circuit supplies the first control signal to each of the sub-drive circuits based on the input signal and a select signal.

A marked-up copy of the amended claims is attached as required under 37 CFR §1.121.

Please add new claims 19-27, as follows:

19. (New) The method according to claim 1, wherein the first output signal generating step includes generating the first output signal that has a gentle waveform in accordance with an input signal having a sharp waveform.

20. (New) The method according to claim 2, wherein the first output signal generating step includes generating the first output signal that has a gentle waveform in accordance with an input signal having a sharp waveform.

21 (New) The output buffer circuit according to claim 5, wherein the first drive circuit receives an input signal having a sharp waveform and generates the first output signal that has a gentle waveform.

22. (New) The output buffer circuit according to claim 5, further comprising a delay circuit, connected to the output terminal, for delaying the first output signal and generating a delayed output signal.

23. (New) A method of controlling an output buffer circuit comprising first and second drive circuits, the first drive circuit including a first output transistor of a first type and a second output transistor of a second type, the second drive circuit including a

third output transistor of the first type and a fourth output transistor of the second type, the third and fourth output transistors having lower impedances than the first and second output transistors, the method comprising the steps of:

generating a first output signal in accordance with the input signal by turning on the first transistor of the first drive circuit; and

driving the second drive circuit to generated a second output signal by turning on the third transistor of the second drive circuit after the first output signal is changed by a predetermined amount by the first drive circuit.

24. (New) The method according to claim 23, wherein the first output signal generating step includes generating the first output signal that has a gentle waveform in accordance with an input signal having a sharp waveform.

25. (New) An output buffer circuit comprising:

a first drive circuit including a first transistor of a first type and a second output transistor of a second type which are connected to an output terminal, wherein the first and second transistors receive an input signal and generate a first output signal by turning on the first transistor or the second transistor;

a second drive circuit including a third transistor of the first type and a fourth transistor of the second type which are connected to the output terminal, wherein the third and fourth output transistors have lower impedances than the first and second output transistors and generate a second output signal; and

a first control circuit, connected to the second drive circuit, for generating a first control signal for turning on the third transistor on the basis of the input signal and the